THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JUERGEN ZIMMERMANN and WALTER GROTE

Appeal No. 1998-0476
Application 08/397,157

ON BRIEF

Before THOMAS, HECKER and DIXON, ***Administrative Patent Judges***.

HECKER, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 7 through 13. Claims 8 through 12 were canceled by an amendment after final rejection, paper no. 8, and claim 13 was canceled by a supplemental amendment, paper

no. 16. Claim 7 is the sole claim remaining on appeal.

The invention relates to a microcomputer which operates selectively with a non-volatile memory (ROM) and a volatile memory (RAM). A monitoring circuit must be periodically reset, when using the ROM or the RAM, otherwise the microcomputer will be automatically reset. Haphazard changes of the RAM content (for example due to interfering E.M.C. radiation, noise) may allow the monitoring circuit to be reset even though the program flow is irregular. The invention provides for suppression of signals to the monitoring circuit so that it may not be reset automatically when operating the RAM mode.

Sole claim 7 is reproduced as follows:

7. A microcomputer, comprising a central processing unit; a non-volatile memory and a volatile memory usable as a [sic] program memories, so that programs executable by said central processing unit are readable into said memories; input/output unit; a monitoring circuit effecting a resetting of the microcomputer when it does not receive any monitoring signal for a predetermined time, the microcomputer operating in at least two different operating states so as to execute a program in said volatile memory in a second operating state; and means for suppressing monitoring signals which are active if the microcomputer is operating in said second operating state; and means for switching the microcomputer from time to

time from said second operating state to said first operating state in which outputting of the monitoring signals is not suppressed and then a monitoring signal is outputted.

The Examiner relies on the following reference:

MOTOROLA Semiconductor Technical Data, "Technical Summary 32-Bit Microcontroller", 1992, MC68F333 TS/D, pp. 3-7, 28-30, 100-102 and 110. (MOTOROLA)

Claim 7 stands rejected under 35 U.S.C. § 101 as lacking patentable utility; under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellants regard as the invention; and under 35 U.S.C. § 103 as being unpatentable over MOTOROLA.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

After a careful review of the evidence before us, we will not sustain the rejection of claim 7 under 35 U.S.C. § 101, 35 U.S.C. § 112, second paragraph, or 35 U.S.C. § 103.

Rejection under 35 U.S.C. § 101

The Examiner contends that the microcomputer of

claim 7 “cannot be utilized” because it repetitively resets itself each “predetermined time” when operating in the RAM mode (answer-pages 3 and 4).

Appellants argue that the microcomputer can be utilized because the microcomputer is switched to the ROM mode “from time to time”, and thus will not reset (brief-pages 14 and 15).

We agree with Appellants for the following reason. As Appellants have noted, the microcomputer is switched to the ROM mode “from time to time”. When in the ROM mode, the signals to the monitoring circuit are not suppressed. Thus the monitoring circuit is automatically reset, and will not overflow. If the monitoring circuit does not overflow, the microcomputer will not be reset, and **can be utilized**.

More specifically, looking at Figure 4, step 36 activates the application function that was loaded into the RAM in step 33. Step 36 is expanded in Figure 5. Here, we

see the switch to RAM mode at step 41 (thus monitor circuit resetting is suppressed). At step 44 the monitor circuit is refreshed. This refreshing is accomplished via a resetting subroutine. This subroutine is shown in Figure 6. At step 50, the microcomputer is switched back to the ROM mode. We note that the ROM mode allows the monitor circuit to be reset, i.e., the signals are not

suppressed. This is the "switching the microcomputer from time to time" recited in claim 7. Resetting of the monitor circuit is accomplished at step 53, the microcomputer is switched back to the RAM mode at step 54, and (back to Figure 5) after refresh step 44, the microcomputer is switched back to ROM at step 47. At step 48, the microcomputer returns to the main program, step 36 in Figure 4.

Thus, we find the claimed invention to have utility, and we will not sustain the Examiner's 35 U.S.C. § 101 rejection.

Rejection under 35 U.S.C. § 112

The Examiner believes claim 7 is indefinite because, as noted in the 35 U.S.C. § 101 rejection, the "predetermined period" would result in continuous resetting of the microcomputer. Such a result does not particularly point out and distinctly claim the invention to the Examiner, and is thus confusing. (Answer-pages 5 and 6.)

Appellants argue that their explanation regarding utility takes care of the 35 U.S.C. § 112 issues (brief-page 15).

We agree with Appellants. Since the invention of claim 7 has been shown to have utility, in that the microcomputer does not continue to reset, the claim does particularly point out and distinctly claim the invention, and there is no confusion.

The Examiner is correct in that there is no specific recitation of a "predetermined time" in the specification. However, there are several operations recited in the specification that take place within a predetermined time. The monitoring circuit has an internal time counter which must be reset within a predetermined time (page 6, lines 9-12).

Flag 22 is set for a “certain time”, page 8, lines 19 and 20. Thus, there could be some confusion as to what the claimed “predetermined time” relates to in the specification. However, considering the context of the claim language, Appellants’ explanation in the brief removes any possible confusion. This, along with Appellants’ explanation in the brief of what is meant by “switching the microcomputer from time to time”, make it clear what Appellants regard as their invention.

Accordingly, we will not sustain the Examiner’s 35 U.S.C. § 112 rejection of claim 7.

Rejection under 35 U.S.C. § 103

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983).

"Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984)).

The Examiner reasons that MOTOROLA teaches the claimed invention except for "suppressing those monitoring signals which are active if the microcomputer is operating to execute a program from the RAM." (Answer-page 8.) The Examiner continues by taking Official Notice

> (a) that suppressing (concealing or subduing) those irregular (faulty or erratic) signals, which have emerged (directly or indirectly) due to radiation (or noise), so as to prevent undesirable consequences is notoriously old and well known in the art, and
>
> (b) that it is a common sense that a monitoring signal would go through a path if it is not suppressed. (Answer-page 9.)

The Examiner states the reasons why it would have been obvious to have modified MOTOROLA, at the bottom of page 9 of the answer.

Simply put, we find no basis for the Examiner's stated reasons to modify Motorola, or the facts taken Official Notice thereof. Both of the Examiner's statements sound very much like the language of Appellants' disclosure.

Appellants argue that MOTOROLA gives no hint of a difference in operation while in the ROM or RAM mode, and makes no mention of suppressing signals to the monitor circuit (brief-page 15). Applicants contend that even if it were known to suppress irregular signals, the solution of switching back and forth between the two operational modes would not have been obvious (brief-page 16).

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902,

USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

As pointed out above, the Examiner has presented no evidence or convincing line of reasoning that a noise problem was known, that RAM's are particularly sensitive to such noise, that a solution to the noise problem would be to suppress the operation of a monitor circuit only during a RAM mode, and that suppression can be successfully accomplished by switching back and forth between the ROM and RAM modes. Since there is no evidence in the record that the prior art suggested the desirability of such a modification, we will not sustain the Examiner's 35 U.S.C. § 103 rejection of claim 7.

We have not sustained the rejection of claim 7 under 35 U.S.C. § 101, 35 U.S.C. § 112 or 35 U.S.C. § 103.

Accordingly, the Examiner's decision is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
STUART N. HECKER Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH L. DIXON Administrative Patent Judge	)	

snh/ki

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